Jpn. J. Appl. Phys. Vol. 40 (2001) pp. 1199–1208
Part 1, No. 3A, March 2001

Four-Thin Film Transistor Pixel Electrode Circuits for Active-Matrix Organic Light-Emitting Displays

Yi HE*, Reiji HATTORI† and Jerzy KANICKI‡

Solid-State Electronics Laboratory, Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, MI 48109, USA

(Received June 2, 2000; accepted for publication November 13, 2000)

Constant-current, four-thin-film-transistor (TFT) pixel electrode circuits, based on hydrogenated amorphous silicon (a-Si:H) TFT technology for active-matrix organic light-emitting displays (AM-OLEDs), have been designed, fabricated, and characterized. Experimental results indicate that continuous pixel electrode excitation can be achieved with these circuits. The pixel electrode circuits use a current driver to automatically adjust their current level for threshold voltage shifts of both the organic light-emitting devices and the drive TFT. Consequently, these pixel electrode circuits have excellent electrical reliability even when a large threshold voltage shift is present. A high output current level and a good output-input current linearity have been demonstrated with these circuits.

KEYWORDS: thin-film-transistor, active-matrix, amorphous silicon, organic light-emitting devices, circuit, luminance, quantum efficiency

1. Introduction

The rapid development of organic light-emitting devices (OLEDs) has made possible their application to high-resolution large-area flat panel displays. Such high-resolution displays require thin-film-transistor (TFT) based active-matrix (AM) driving schemes to reduce their power dissipation. Over the past few years, much effort has been made to develop AM driving techniques for organic light-emitting displays.[1–4] Pixel electrode driving schemes based on one-TFT,[1] two-TFT,[2,3] and four-TFT[4] circuits have been proposed. Today, it is well established that the one-TFT pixel electrode configuration[1] cannot be used for AM-OLED because continuous excitation during the entire frame period cannot be achieved with this type of pixel circuit. Continuous pixel electrode excitation can be achieved by a two-TFT configuration.[2,3] However, in this type of pixel electrode circuit, non-negligible threshold voltage (V_{th}) variation of the drive TFT, due to TFT process variation or long-term operation, can occur and cause output current level variation over the display panel. As a result, the light emission intensity of OLED and AM-OLED brightness can change accordingly, which may not be acceptable for certain applications. The previously proposed four-TFT pixel configuration,[4] although partially compensating for V_{th} variation, uses four control lines and its driving scheme is too complicated for practical use. It should also be noted that so far, the proposed four-TFT pixel electrode circuit has been based on polysilicon TFT technology,[2–4] which may not be a cost-effective production technology in comparison with the well-established amorphous silicon (a-Si) TFT technology developed for AM-liquid crystal displays (AM-LCDs).

In this paper, we describe the current-source four-TFT pixel electrode circuits based on amorphous silicon TFT technology. The developed circuits are extensively characterized for different sets of circuit parameters. We clearly demonstrate, for the first time, that this type of pixel electrode circuit can provide continuous current flow even after the select line signal is turned off. In addition, current flow can be fully adjusted for the current-voltage characteristic variation of the TFTs and OLEDs. Consequently, these pixel circuits are able to maintain a constant level of current flow and have high electrical reliability. Also, these pixel electrode circuits have only two control lines and, as a result, their driving schemes are simple. Finally, two improved circuits are proposed to further enhance pixel circuit electrical performance. Pixel electrode circuit simulations and experimental results indicate that the proposed circuits are acceptable for AM-OLEDs.

2. Pixel Electrode Circuit Schematic and Operation

Figure 1(a) shows the schematic of the equivalent constant current four-TFT pixel electrode circuit. T1 and T2 are the switching transistors. T3 is the drive TFT while T4 serves as a one-direction diode that only allows current flow from V_{DD} (common source) line to the OLED. This circuit has four external terminals: V_{select}, I_{data}, V_{DD}, and ground. The select line voltage signal, V_{select}, and the source line voltage signal, V_{DD}, are pulsed and constant voltage signals, respectively. The data line signal, I_{data}, is an adjustable *current* signal to be provided by an external current driver. All signals (V_{select}, I_{data}, and V_{DD}) are provided externally, and the ground terminal is the cathode (metal electron injecting electrode) of the OLED. Figure 1(b) shows an example of the operational waveforms that can be used for different signals. The operation of this circuit is described as follows:

ON state: When the select line (V_{select}) signal is high (H), both T1 and T2 are turned ON. The data line signal (I_{data}) then passes through T1 and T2 and sets both the drain and gate voltages of T3. Consequently, the potentials at nodes A and B will allow the data current (I_{data}) to pass through T3. T3 is working in the saturation region, *e.g.*, $V_{DS} > V_{GS} - V_{th}$ (threshold voltage). V_{DD} must be chosen to be lower than the T3 drain voltage (V_D) during the ON state to ensure that no current flows through T4 from V_{DD}. Therefore, in this case, the current flowing though T3 is equal to I_{data}. This current,

*Present address: One AMD Place, P.O. Box 3453, MS 177, Sunnyvale, CA 94088-3453, USA.
†Present address: Department of Electronic Device Engineering, Graduate School of Information Science and Electrical Engineering, Kyushu University, Hakozaki 6-10-1, Higashi-ku, Fukuoka 812-8581, Japan.
‡Corresponding author: kanicki@eecs.umich.edu

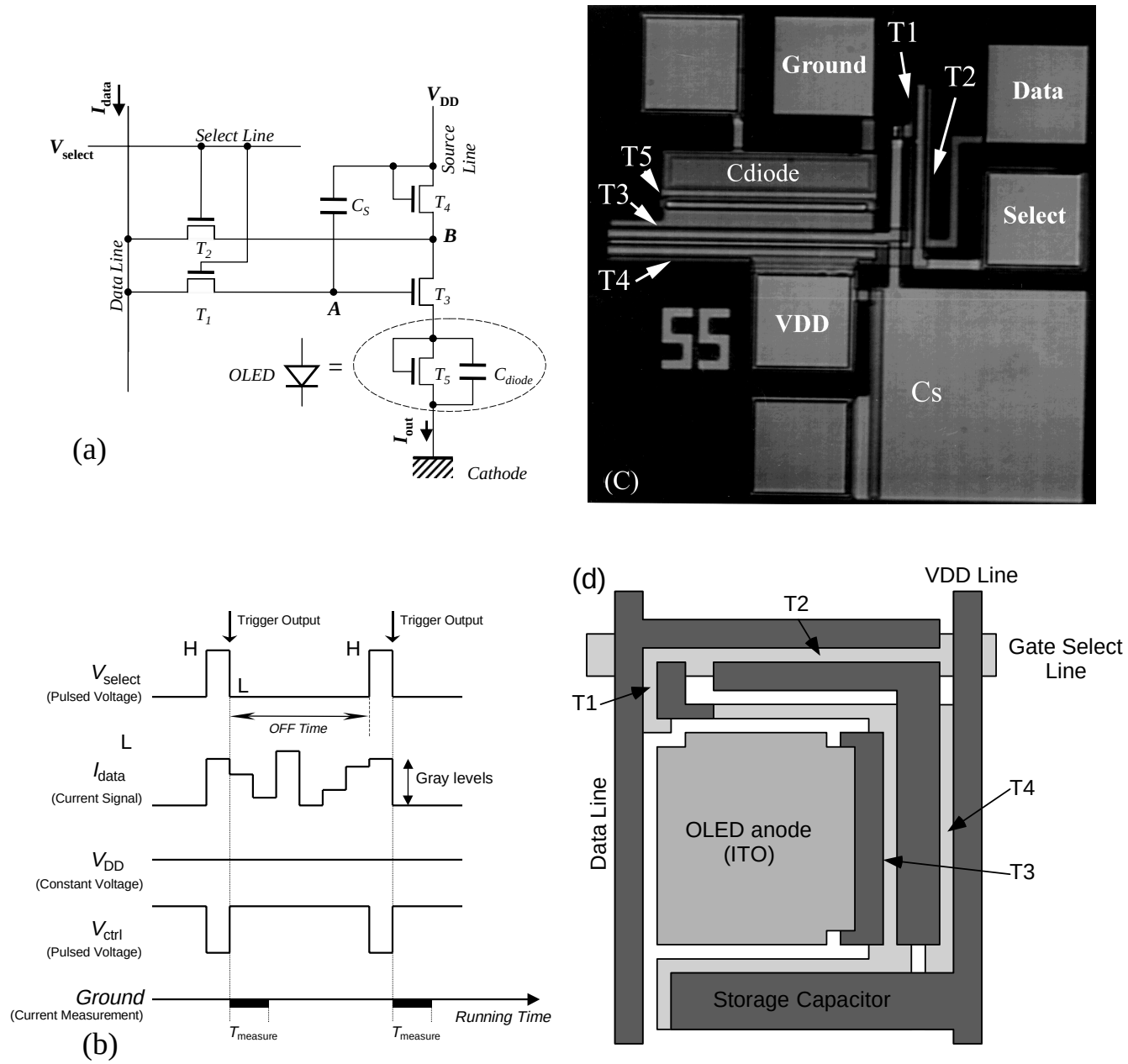

Fig. 1. (a) Schematic representation of the four-TFT pixel electrode circuit. (b) Example of the operation waveforms that can be used for different external terminals. (c) Top view of the four-TFT pixel electrode circuit fabricated in our laboratory. (d) Schematic top view of the four-TFT pixel electrode circuit. C_s represents the storage capacitor. T1, T2, ... T5 represent TFT1, TFT2, ... TFT5, respectively.

applied to the OLED anode (ITO electrode), will turn on the OLED and reach the ground pad (OLED cathode). The OLED light emission brightness will depend on the applied current level that can be modulated, as shown in Fig. 1(b).

OFF state: When the pixel electrode circuit is de-selected and the select line signal is low (L), both T1 and T2 are OFF. The T3 gate voltage (V_G), however, should be maintained high by charges stored in the storage capacitor (C_s) during pixel electrode ON state. During OFF state, the T3 drain voltage will drop to a lower value and T4 will be turned on to maintain the same output current level. This time, the current will flow from V_{DD} to T3 via T4. If the T3 gate voltage is maintained and T3 is operated in the saturation region, the output current level would be equal to I_{data}. Therefore, the current flowing through OLED is expected to be maintained constant.

Automatic adjustment: If the drive TFT (T3) threshold voltage changes and if this change is not larger than the amplitude of V_{select} during pixel electrode circuit operation, V_G of T3 must be changed accordingly to ensure the same output current level. This is achieved through automatic adjustment of the current signal (I_{data}) during the ON state. Therefore, the gate voltage of T3 is always adjusted to maintain the data current (I_{data}) level at about the same level, regardless of the TFT threshold voltage value. Hence, the local V_{th} variation of the drive TFT will not affect the output current (I_{out}) level. The threshold voltage shifts of other TFTs will not have a major impact on the output current level, because they are not

involved in controlling the current output in this pixel electrode circuit.

These above arguments also hold if the OLED current-voltage characteristic shifts with time, which usually happens after long-term OLED operation. Consequently, this pixel electrode circuit can provide constant current flow even if local variations of the OLED characteristics occur.

The gray level of this pixel electrode circuit is controlled by adjusting the data current level [Fig. 1(b)]. As discussed above, the output current is expected to be the same as the data current in both ON and OFF states. Therefore, the output current level is directly controlled by the data current from the data line. Since OLED brightness is usually proportional to the current density passing through it,[5] different output currents will generate different OLED brightness levels that can be used to control the display gray levels.

3. Experimental

To verify pixel electrode circuit functionality, we have designed and built this circuit based on a-Si:H TFT technology. The four-TFT pixel circuit fabricated during this study is shown in Fig. 1(c). In this figure, the OLED structure is represented by a combination of TFT (T5) and a parallel capacitance (C_{diode}) [Fig. 1(a)]. The geometrical sizes of T5 and C_{diode} have been optimized to ensure that under forward bias condition, the current flow through the T5-C_{diode} combination is similar to that expected in the fabricated OLED. Indeed, T5, whose gate electrode is connected to its drain electrode, shows a rectifying characteristic.[6] The channel length for all TFTs is 6 μm.

The pixel electrode circuit was fabricated on a Corning 1737 $6'' \times 6''$ square glass substrate using a conventional inverted-staggered back-channel-etch process.[7] First, a 1000-Å-thick chromium layer was deposited on Corning 1737 glass by the sputtering method and patterned to form the gate electrodes of all five TFTs and the bottom electrode of the storage capacitor (C_s). A-SiN$_x$:H (3000 Å), intrinsic a-Si:H (2000 Å), and n$^+$ a-Si:H (500 Å) layers were then deposited sequentially by the plasma-enhanced chemical vapor deposition (PECVD) technique. After the patterning of the active area (a-Si:H island) for all TFTs and the gate via opening for T3, T4, and T5, 2000-Å-thick molybdenum was deposited by the sputtering method and patterned to form the source-drain electrodes of all five TFTs and the top electrode of the storage capacitor. The interconnects (for example, T1 source to T3 gate, etc.) between different TFTs were formed at the same time. The TFT back channel was reactive-ion etched (RIE) using the dry etching process. Then, a-SiN$_x$:H (3000 Å) was deposited on top to passivate the pixel circuit. The via in the passivation layer was opened afterwards. Finally, the ITO electrode was sputtered, annealed and etched. When OLED is incorporated into this pixel electrode circuit, the T5 and C_{diode} structure can be omitted, the OLED structure will be fabricated on top of the ITO electrode, and light will be emitted down through the ITO layer. Figure 1(d) illustrates the schematic representation of the fabricated pixel electrode circuit.

The electrical properties of the pixel circuit were evaluated using a probe station. Data (constant current, I_{data}) and source line (constant voltage, $V_{\text{DD}} = 9$ V) signals were supplied by HP 4156A semiconductor analyzer. The select line signal (pulsed voltage, V_{select}) was supplied by a Keithley 237 source-measure unit with an ON voltage = 25 V, an OFF voltage = 0 V, and a duty cycle of 10% (ON time: 100 ms, period: 1000 ms). The output current (I_{out}) of this circuit was measured by the HP semiconductor analyzer after input data current (I_{data}) and source line voltage (V_{DD}) were turned off, i.e., after the pixel electrode circuit was de-selected. This will enable verification of the pixel electrode circuit's ability to provide continuous excitation. The sampling of the output current was triggered by the falling edge of the select pulse voltage signal to ensure that data were collected after the pixel circuit was turned off. The typical sampling time for each data point was found to be $\sim$ 2–3 ms using the HP 4156A semiconductor analyzer. Therefore, all measurements were performed in the OFF state, *e.g.*, when the V_{select} signal was low. The experimental noise was below 10 pA.

4. Experimental Results and Discussions

4.1 I_{out}–I_{data} characteristics

During the ON state, The output current (I_{out}) measured at the ground pad (OLED cathode) approximately equals the data current (I_{data}) provided by the current source from the data line. However, as discussed previously, continuous pixel excitation is necessary for an AM-OLED driving circuit. To verify the circuit's ability to continuously supply the pixel electrode current, the output current in the OFF state was investigated.

Figure 2(a) illustrates the output current in the OFF state versus data current characteristics of the four-TFT pixel circuit at different V_{DD} voltages for a storage capacitor of $\sim$ 6.61 pF. All the characteristics were measured after V_{select} was switched off from 25 to 0 V and the pixel electrode circuit was de-selected. It is clear that continuous pixel electrode excitation was achieved in this pixel circuit. For all V_{DD} voltages, the output current level increases monotonically with the data current, indicating that the output current level is solely controlled by the data current for given V_{DD} voltage and storage capacitor values. This characteristic will enable the control of AM-OLED gray scale solely by the data current. In addition, a higher output current level can be achieved with higher V_{DD} values. Note that when V_{DD} was high, the output current was not zero even if the input data current was zero. This is due to the fact that even when I_{data} is zero, the T4 source voltage [point B in Fig. 1(a)] is not zero. Since I_{data} is zero, the voltage at point A will be equal to the voltage at point B. This will keep T3 slightly ON to allow a small amount of current to pass through. When V_{DD} voltage is higher, the voltage at point A will also be higher, leading to an even larger output current.

In Fig. 2(b), the output current characteristics in the OFF state for different C_s are plotted together at a given V_{DD} voltage (9 V). These experimental results verified that a larger output current level could be achieved for a larger size of the storage capacitor. The I_{out} values for $I_{\text{data}} = 0.2\,\mu$A in the OFF state are listed in Table I. From this table, we can conclude that the output current (I_{out}) decreases with respect to the input data current (I_{data}) when the pixel circuit is switched from ON to OFF state. The data listed in this table were measured using the follow-

Table I. Output current and storage capacitor values deduced from Fig. 2(b). The ΔV values were calculated using eq. (8).

Circuit no.	Storage capacitor (pF)	I_{out} (ON)* (μA)	I_{out} (OFF) (μA)	ΔI_{out} (μA)	ΔV (V)
1	0.052	0.20	0.03	0.17	0.85
2	0.41	0.20	0.04	0.16	0.71
3	0.83	0.20	0.07	0.13	0.55
4	1.65	0.20	0.09	0.11	0.44
5	3.31	0.20	0.12	0.08	0.32
6	6.61	0.20	0.15	0.05	0.17

*$I_{out}(ON) = I_{data}$; $\Delta I_{out} = I_{out}(ON) - I_{out}(OFF)$.

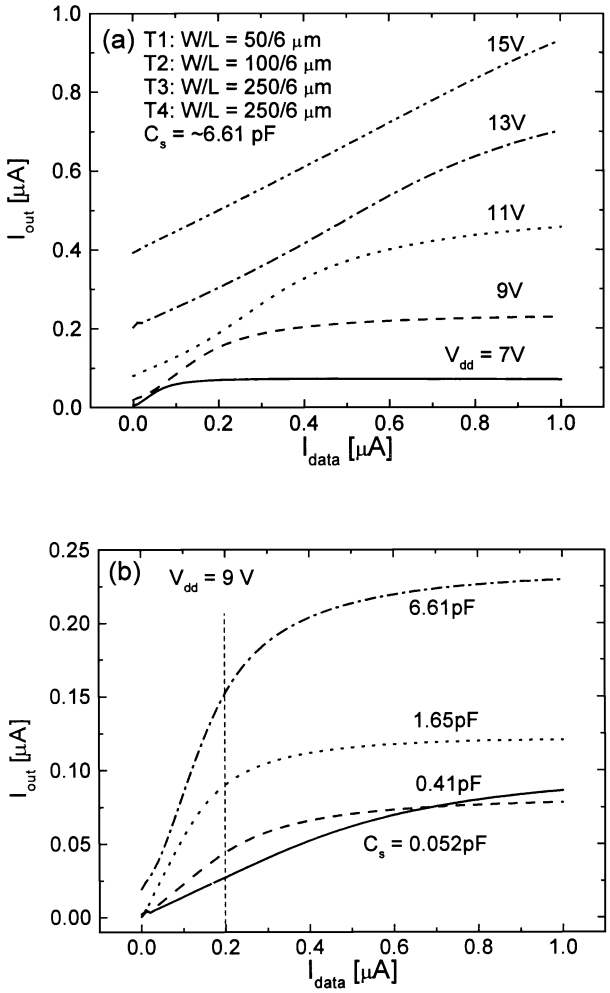

Fig. 2. (a) Output current versus data current characteristics of the four-TFT pixel electrode circuits at different V_{DD} voltages for a storage capacitor size of $\sim$ 6.61 pF. (b) Output currents at $V_{DD} = 9$ V for different C_s. All curves were measured during OFF state of the pixel electrode circuit.

ing parameters: $V_{select} = 25\,V \rightarrow 0\,V$, $V_{DD} = 9\,V$, and $I_{data} = 0.2\,\mu A$. Also, the TFTs have the following W/L ratios: T1 $W/L = 50/6\,\mu m$, T2 $W/L = 100/6\,\mu m$, T3 $W/L = 250/6\,\mu m$, T4 $W/L = 250/6\,\mu m$, and T5 (OLED-emulating TFT) $W/L = 200/6\,\mu m$. The output current level decrease observed for higher I_{data} values is mainly due to the gate voltage decrease induced by the parasitic capacitor.

In general, the TFT parasitic capacitor (C_p) is due to the overlap between TFT source/drain and gate electrodes, as shown schematically in Figs. 3(a) and 3(b). It should be noted that all TFTs shown in Fig. 1(a) have their own parasitic capacitors. Among them, the T1 parasitic capacitor (C_{p1}) will cause a T3 gate potential drop when V_{select} is switched from 25 to 0 V. Figure 3(c) illustrates the equivalent pixel circuit at node A shown in Fig. 1(a). When V_{select} is 25 V, node A (T3 gate) is charged up to the data line voltage (V_{data}) by I_{data}. This voltage value is determined by the present current source voltage. Thus, the charge stored at node A is

$$Q = C_{p1}(V_{data} - V_{select(ON)}) + C_{gd}(V_{data} - V_d) + C_{gb}(V_{data} - V_{a\text{-}Si})C_{gs}(V_{data} - V_s) + C_s(V_{data} - V_{dd}), \quad (1)$$

where C_{p1} is the T1 parasitic capacitor; and C_{gd} and C_{gs} are the T3 gate-to-drain and gate-to-source capacitors, respectively. If the source/gate and the drain/gate overlaps of T3 are identical, $C_{gd} = C_{gs} = C_{p3}$, where C_{p3} represents the T3 parasitic capacitance. C_{gb} is the capacitance associated with the gate over the field region,[8] and is equal to the gate oxide capacitor ($C_{gb} = C_{ox}$). V_d and V_s are the T3 drain and source voltages. $V_{a\text{-}Si}$ is the equivalent T3 field region potential. Then, the above equation can be simplified as

$$Q = C_{p1}(V_{data} - V_{select(ON)}) + C_{p3}(2V_{data} - V_d - V_s) + C_{ox}(V_{data} - V_{a\text{-}Si}) + C_s(V_{data} - V_{dd}). \quad (2)$$

When V_{select} is switched to 0 V, the charge stored at node A is

$$Q' = C_{p1}V' + C_{p3}(2V' - V'_d - V'_s) + C'_{gb}(V' - V'_{a\text{-}Si}) + C_s(V' - V_{dd}), \quad (3)$$

where V' represents the potential at node A after V_{select} is switched from 25 to 0 V. After this switching step, if T3 still operates in the saturation region, C'_{gb} would remain the same (C_{ox}). Assuming that the T3 field region ($V_{a\text{-}Si}$) and the T3 drain and source (the potential applied to OLED) potential changes are negligible after each switching, eq. (3) can be rewritten as

$$Q' = C_{p1}V' + C_{p3}(2V' - V_d - V_s) + C'_{ox}(V' - V_{a\text{-}Si}) + C_s(V' - V_{dd}). \quad (4)$$

Q' would be equal to Q if there were no charge leakage from node A back to the data line through T1 in the OFF state. Therefore, by substituting of eq. (4) into eq. (2) and replacing ($V_{data} - V'$) by ΔV, we obtain

$$\Delta V = \frac{C_{p1}\Delta V_{select}}{C_{p1} + 2C_{p3} + C_{ox} + C_s}. \quad (5)$$

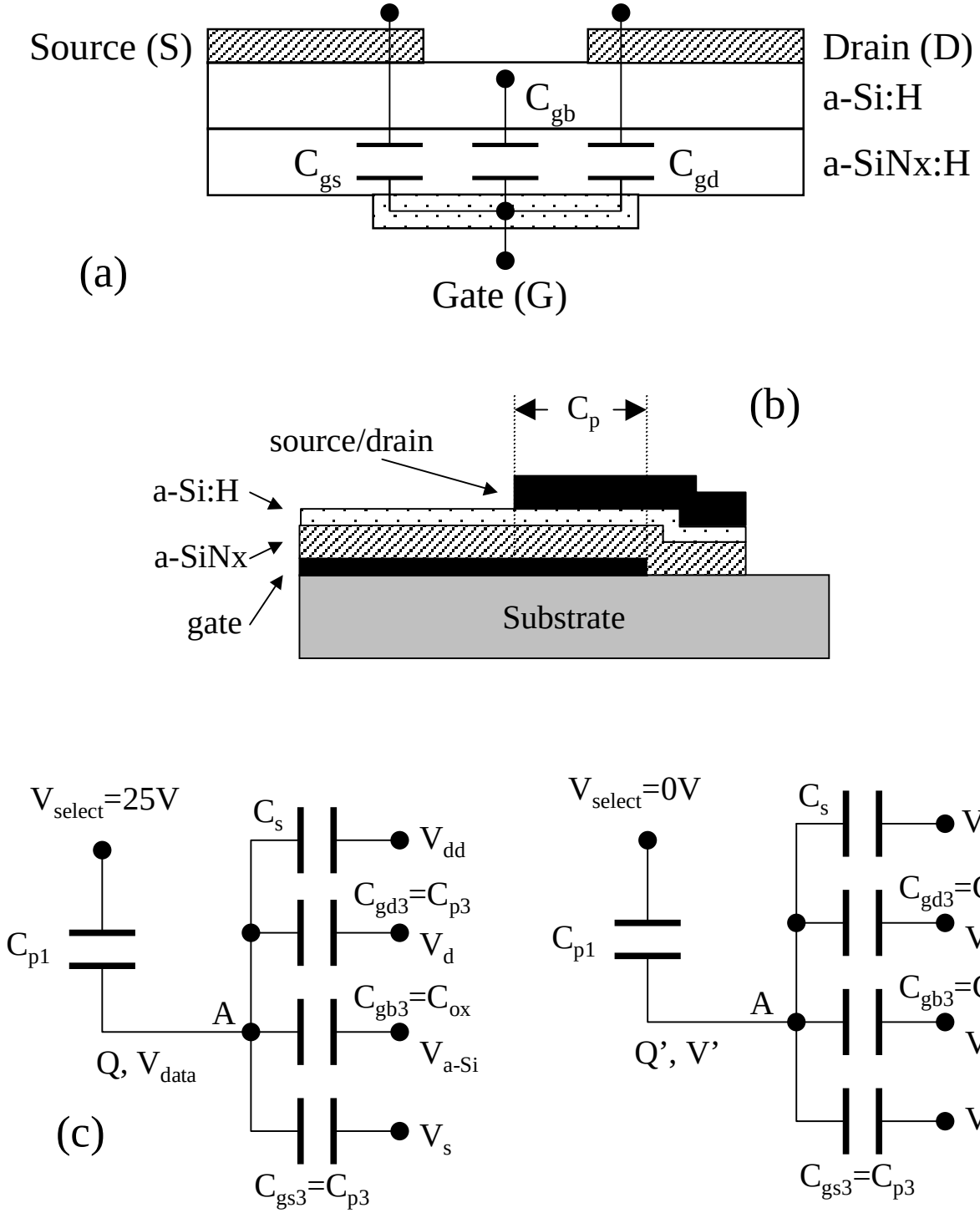

Fig. 3. (a) Schematic representation of TFT. (b) Cross-sectional view of the TFT near source/drain–gate electrodes; C_p represents the TFT parasitic capacitor. (c) The equivalent circuit at node A of Fig. 1(a).

The inverse of eq. (5) gives

$$1/\Delta V = \frac{C_{p1} + 2C_{p3} + C_{ox} + C_s}{C_{p1}\Delta V_{select}} = \frac{1}{C_{p1}\Delta V_{select}} C_s + \frac{C_{p1} + 2C_{p3} + C_{ox}}{C_{p1}\Delta V_{select}}. \quad (6)$$

The second term on the right-hand side of eq. (6) is a constant for fixed V_{select} and pixel electrode circuit parameters. Therefore, the relationship between $1/\Delta V$ and the storage capacitor should be linear. In order to use eq. (6) to analyze the data given in Table I, the gate voltages responsible for the output current drops must be derived. Assuming that T3 (drive TFT) is in the saturation region before and after pixel electrode circuit switching, the T3 output current should follow the equation

$$I_{ds} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2, \quad (7a)$$

where I_{ds} is the drain-to-source current; μ is the field-effect mobility; W and L are the channel width and length, respectively; and V_{gs} and V_{th} are the gate-to-source and threshold voltages, respectively. Rewriting the above equation to show

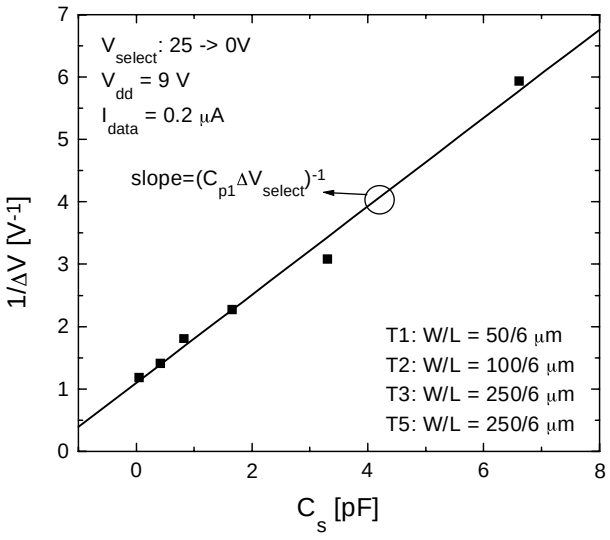

Fig. 4. Calculated ΔV as a function of the storage capacitor (—). The calculated ΔV values (■) from experimental data are also shown.

V_{gs} in the left term, we obtain

$$V_{gs} = V_{th} + \sqrt{\frac{2L}{\mu C_{ox} W} I_{ds}}. \tag{7b}$$

Because data collection takes only $\sim$ 2–3 ms after pixel circuit switching, it is expected that no significant threshold voltage shift of T3 will take place. Therefore, in general, the gate voltage variation should obey the following equation:

$$\Delta V = V_{gs} - V'_{gs} = \left(\frac{2L}{\mu C_{ox} W}\right)^{1/2} (\sqrt{I_{on}} - \sqrt{I_{off}}), \tag{8}$$

where V'_{gs} is the T3 gate-to-source voltage after the pixel circuit switching step. $I_{on} = I_{out}(\text{ON})$, $I_{off} = I_{out}(\text{OFF})$, $\mu \approx 0.26\,\text{cm}^2/\text{V·s}$, $C_{ox} \approx 2.07 \times 10^{-8}\,\text{F/cm}^2$, $L = 6\,\mu\text{m}$, $W = 250\,\mu\text{m}$ for the data listed in Table I.

Figure 4 shows the variation of the inverse of the gate voltage (ΔV), derived from eq. (8) based on the data given in Table I, as a function of the storage capacitor. It is clear from this figure that the inverse of the gate voltage decreases linearly with the size of the storage capacitor, as suggested by eq. (6). According to eq. (6), the slope [$(0.71 \pm 0.04) \times 10^{12}\,\text{F}^{-1}\cdot\text{V}^{-1}$] of the straight fit line should be equal to $1/C_{p1}\Delta V_{select}$. Thus, from this slope, we can calculate the T1 parasitic capacitor value as

$$C_{p1} = \frac{1}{0.71 \times 10^{12} \Delta V_{select}} \approx 56.3\,\text{fF}, \tag{9}$$

where $\Delta V_{select} = 25\,\text{V}$. If we take into consideration film thickness variation, dielectric constant uncertainty, and misalignment associated with the photo-process during TFT fabrication, the parasitic capacitance value ($= \varepsilon_r \varepsilon_0 W L_{overlap}/t$, $\varepsilon_r \approx 7$, $t \approx 3000$Å), calculated directly from the design parameters, for T1 ($W/L = 50/6\,\mu\text{m}$, $L_{overlap} = 2\,\mu\text{m}$) is $\sim 20.7 \pm 20\,\text{fF}$. This value is comparable in magnitude to the parasitic capacitance derived from Fig. 4. Therefore, the above analyses provide a good justification for the origin of the T3 gate voltage reduction associated with the T1 parasitic capacitor. The observed deviation between theoretical and measured results may also be due to the following:

a) Some of the assumptions made during the derivation of eq. (6) may not hold during pixel circuit operation. For example, during the derivation of eq. (5), it is assumed that the T3 source potential (the potential applied to OLED) remains at the same level after pixel circuit switching step. This assumption cannot be 100% correct because the current (I_{out}) flowing through OLED changes. The current change is a direct result of the OLED bias change. Therefore, the T3 source potential cannot remain at the same level if an output current change is observed. In many cases, such a potential change could be very small, particularly in the high-current regions where a slight voltage change induces a large current fluctuation. In the case of $I_{out} = 0.2\,\mu\text{A}$, however, this potential change may not be sufficiently small to be neglected.

b) Other output current reduction mechanisms may be involved. For example, the charge leaks through T1 to the data line, or the T3 (drive TFT) operation point moves from saturation to the linear region after the pixel electrode circuit switching step.

In both cases, the output current level will be further reduced, resulting in a larger calculated C_{p1} value using eq. (6).

According to eq. (6), the Y-axis intercept (1.10 ± 0.12) of the fitted straight line in Fig. 4 corresponds to $(C_{p1} + 2C_{p3} + C_{ox})/(C_{p1}\Delta V_{select})$. Therefore, the C_{p1} value can be also derived from the intercept value if other parameters are known. This calculated C_{p1} value is $\sim$ 19.5 fF, in excellent agreement with the parasitic capacitance value (20.7 fF) calculated above directly from the TFT design parameters.

From the above analysis, it is clear that a certain size of storage capacitor is needed for the four-TFT pixel electrode circuit. In general, a larger C_s is preferred to minimize the reduction of the output current after pixel electrode circuit switching. Also, the V_{DD} voltage must be carefully selected to reduce the output current deviation observed at low data currents.

4.2 Impact of TFT W/L ratios

Figure 5(a) illustrates the influence of the T1 W/L ratio on the output current characteristics in the OFF state. Experimentally, we have observed that a larger output current level can be reached for a larger T1 W/L ratio. However, at the same time, when the T1 W/L ratio was too large, the output current could not reach zero even if the input data current was set to zero. The pixel electrode circuit output current characteristics showed little dependence on the T2 W/L ratio.

Figure 5(b) shows the influence of the T3 (drive TFT) W/L ratio on the output current characteristics in the OFF state. It is clear that for a larger T3 W/L ratio, a higher output current level can be achieved. However, when the T3 W/L ratio was too large, the output current could not reach zero even if the input data current was zero. Figure 5(c) illustrates the transient characteristic of the output current for the four-TFT pixel circuit. The V_{DD} voltage and the input data current were 13 V and 0.2 μA, respectively. From this figure, it is clear that the output current slightly decreased after the pixel electrode circuit was switched OFF, but the output current level remained unchanged for at least 1 second after the select line signal was turned off, indicating a negligible pixel electrode circuit leakage current.

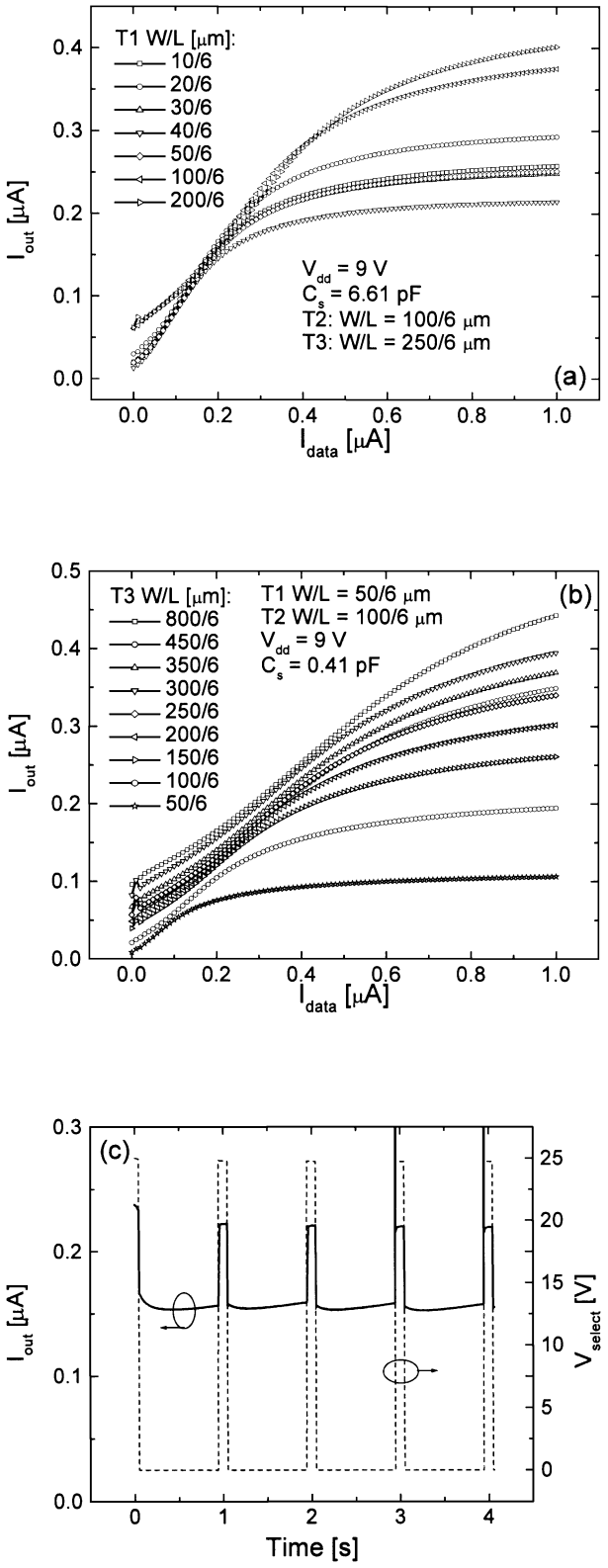

Fig. 5. Influences of (a) T1 W/L ratio and (b) T3 W/L ratio on the output current characteristics of the four-TFT pixel electrode circuit. (c) The transient response of the four-TFT pixel electrode circuit.

Based on our experimental results and pixel electrode circuit analyses, the best set of pixel electrode circuit parameters is listed in Table II for the pixel circuit described above. Further improvement of this pixel circuit will require further process refinement and video-rate test current signals.

Table II. Best pixel electrode circuit parameters to be used for the a-Si:H four-TFT pixel electrode circuit described in this paper.

T1 W/L (μm)	T2 W/L (μm)	T3 W/L (μm)	C_s (pF)	V_{DD} (V)
50/6	200/6	250/6	6.61	9

4.3 Pixel electrode circuit electrical reliability

One basic function of the AM-OLED pixel electrode circuit is to consistently provide a *constant* current for the OLED during the frame period. The experimental results showed that this is indeed the case for the four-TFT pixel circuit and the output current level can simply be adjusted by supplying different data current values. This should allow good control of the AM-OLED gray levels.

However, serious circuit electrical instability may occur due to the drive TFT threshold voltage shift, particularly for the two-TFT circuit.[6] This drive TFT threshold voltage shift can cause a large AM-OLED brightness variation. To study the electrical reliability of this pixel electrode circuit, we have conducted a series of DC bias-temperature-stress (BTS) on the drive TFT (T3) to accelerate the aging process of the pixel electrode circuit. The threshold voltage shift of other TFTs presented in this circuit will not have a major impact on the output current level, because they are not used to control the pixel electrode current output. During BTS, a bias stress voltage of $+20$ V was applied to the T3 gate at room temperature. The best pixel electrode circuit parameters given in Table II were used for pixel circuit electrical reliability evaluation.

Figure 6(a) illustrates the variation of pixel electrode circuit output current characteristics as a function of BTS time. It is clear from this figure that the output current level remained essentially unchanged during BTS up to 10^4 s. Figure 6(b) shows the T3 threshold voltage evolution as a function of BTS time. For a BTS time of 10,000 s, the threshold voltage was shifted by $\sim$ 2.77 V from its initial value. Figure 6(b) also illustrates that the output current changed by only $\sim$ 1% at high input current ($\geq$ 0.5 μA) and by $\sim$ 5% at low input current ($\geq$ 0.1 μA). These results clearly show that this pixel electrode circuit is capable of compensating for the T3 V_{th} variation to ensure a stable, constant pixel output current level. This will allow both good control of the display gray levels and uniform luminance distribution over the entire AM-OLEDs.

5. Improved Four-TFT Pixel Electrode Circuits

In an ideal case, the pixel electrode output current level in the OFF state should be equal to the input data current, as indicated by the ideal line in Fig. 6(a). However, experimental results showed that the output current levels were substantially lower than the ideal case, particularly at high input current levels [Fig. 6(a)]. This deviation from the ideal case may be associated with (a) gate voltage reduction induced by the parasitic capacitor, C_{p1}, as discussed in detail above. The consequence of the gate voltage decrease is the decrease of the T3 output current level. This effect is large at low input current levels, where both V_{gs} and V_{ds} are small; (b) after the pixel electrode circuit is de-selected, the magnitude of the T3 drain voltage will decrease. This voltage drop could produce $V_{ds} < V_{gs} - V_{th}$. As a result, the T3 operating point will shift

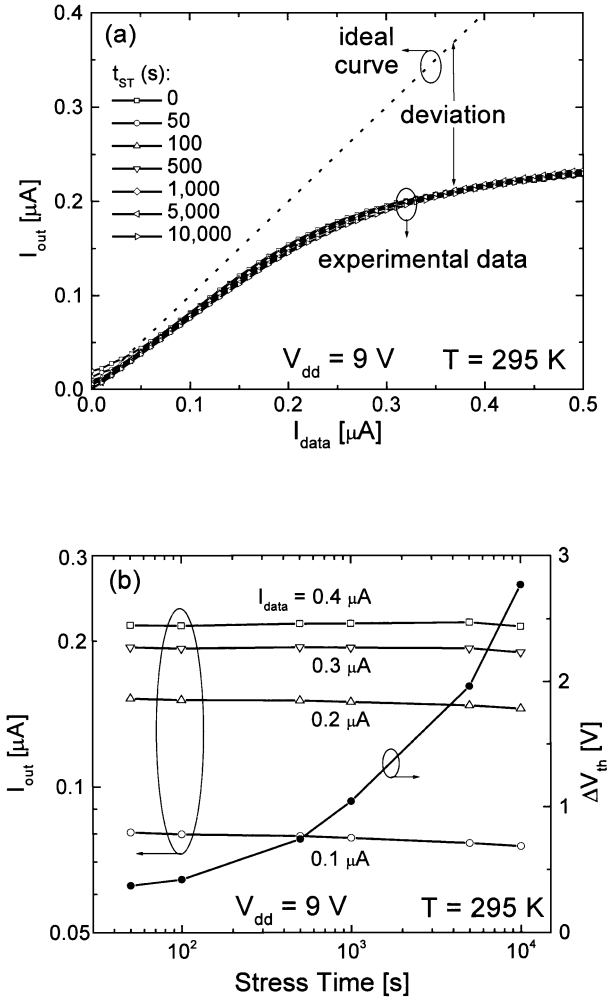

Fig. 6. (a) Impact of BTS on the four-TFT pixel electrode circuit characteristics. (b) BTS time dependence of the threshold voltage and the output current at several data currents, $\Delta V_{th} = V_{th}^{f} - V_{th}^{i}$, where V_{th}^{f} and V_{th}^{i} are the TFT final and initial threshold voltages, respectively.

from the saturation region to the linear region, and the output current (I_{out}) will decrease with respect to I_{data}. This effect will be dominant at high input current levels, where both V_{gs} and V_{ds} of T3 in the ON state are large in comparison with V_{DD}.

The output current deviation can be reduced by increasing the external source line voltage (V_{DD}). A higher V_{DD} will result in larger output current levels (see Fig. 2). However, at the same time, an incorrect output current level can be induced at low input currents, where the T3 drain voltage could be lower than V_{DD}. As a result, current [I_D(T4)] will flow from V_{DD} to T3 via T4 and the total output current $I_{out} = I_{data} + I_D(T4) > I_{data}$. This situation can be seen in both Figs. 2 and 5. For the circuit to work reasonably well at both low and high data current levels, a compromise V_{DD} voltage must be reached. In the case of our four-TFT pixel electrode circuit, $V_{DD} = 9\,V$ seemed to be the best choice (Table II).

However, even at $V_{DD} = 9\,V$, a large deviation and nonlinearity between the output and input currents still exist, and the output current tends to saturate at high currents [Fig. 6(a)]. Therefore, this pixel circuit might not be able to provide a sufficiently large current density if a high OLED brightness is required. To achieve a high output current and a good output-input current linearity, the four-TFT pixel electrode circuit was slightly modified [Fig. 7(a), the top view of this circuit is shown in Fig. 7(d)]. By connecting an extra voltage control line (V_{ctrl}) to the T4 gate electrode, the V_{DD} voltage can now be set at 25 V or higher. During the ON-time, the V_{ctrl} signal is low and T4 is turned off. The data line signal (I_{data}) then passes through T1 and T2 and sets both the drain and gate voltages of T3. Consequently, the potentials at nodes A and B will allow the data current (I_{data}) to pass through T3. T3 is working in the saturation region, *e.g.*, $V_{DS} > V_{GS} - V_{th}$ (threshold voltage). Because T4 is off, no current can flow through it from V_{DD}. Hence, the current flowing though T3 is equal to I_{data}. This current then will turn on T5 (*e.g.*, OLED) and reach the ground. During the OFF time, the V_{ctrl} signal is high to turn on T4, allowing for the current to flow from V_{DD} to T3 via T4. Since V_{DD} now represents a high potential power source, the potential at point B will increase after the pixel circuit is switched from ON to OFF state. The T3 gate voltage is maintained at the previous level by charges stored in the storage capacitor C_s. Therefore, V_{DS} of T3 remains higher than $V_{GS} - V_{th}$ and the TFT remains in the saturation region. Consequently, the pixel output current (I_{out}) is maintained at the same level as that in the ON state. Thus, $I_{out} = I_{data}$.

A closer inspection of this pixel electrode circuit reveals that the signal of the V_{ctrl} terminal is exactly the inverse of the select line signal (V_{select}). Therefore, a two-TFT based inverter can be added to this pixel electrode circuit to replace the V_{ctrl} terminal. This approach, illustrated in Fig. 7(b), will reduce the number of pixel electrode terminals but will increase pixel electrode circuit complexity. However, the two-TFT based inverter does not have to be included in every pixel electrode circuit. Instead, it can be fabricated at the edge of the display panel or included in the driving display circuit to reduce pixel electrode circuit complexity. To achieve the voltage inversion, the geometrical dimensions of T6 and T7 need to be optimized, so that $W_7L_6/L_7W_6 \gg 1$ (W_6, W_7, L_6 and L_7 represent the channel widths and lengths of T6 and T7, respectively.). In the ON state, V_{select} will turn on T1, T2, and T7. T6 is always on because its drain and gate electrodes are connected. Since both T6 and T7 are on, the current flows from V_{DD} to ground through T6 and T7. In equilibrium, T6 and T7 will function as two resistors linked in series, and the gate voltage of T4 at node C will be determined by these two resistor and V_{DD} values. Since the resistance of TFT in the ON state is proportional to its W/L ratio, the T4 gate voltage will be $\sim V_{DD} \times W_6L_7/L_6W_7 \ll V_{DD}$. This voltage can be adjusted to a value smaller than the threshold voltage of T4 by choosing the appropriate W_6, W_7, L_6 and L_7 values. Then T4 will be off and, therefore, no current will flow through T4, as in the case of the V_{ctrl}-line approach. In the OFF state, T1, T2, and T7 will be turned off. The gate voltage of T4 at node C will be set high by V_{DD} through T6. This circuit condition will allow the current to flow from V_{DD} to T3 through T4. Similar to the case of the V_{ctrl}-line approach, V_{DS} of T3 will remain higher than $V_{GS}-V_{th}$, and T3 will still operate in the saturation region. As a result, the pixel electrode output current level will remain constant.

To support the above analysis, circuit simulation was performed using Cadence. The pixel circuit simulation parameters used in this work are summarized in Table III. Note that for the pixel circuit simulation, all the TFT parasitic capac-

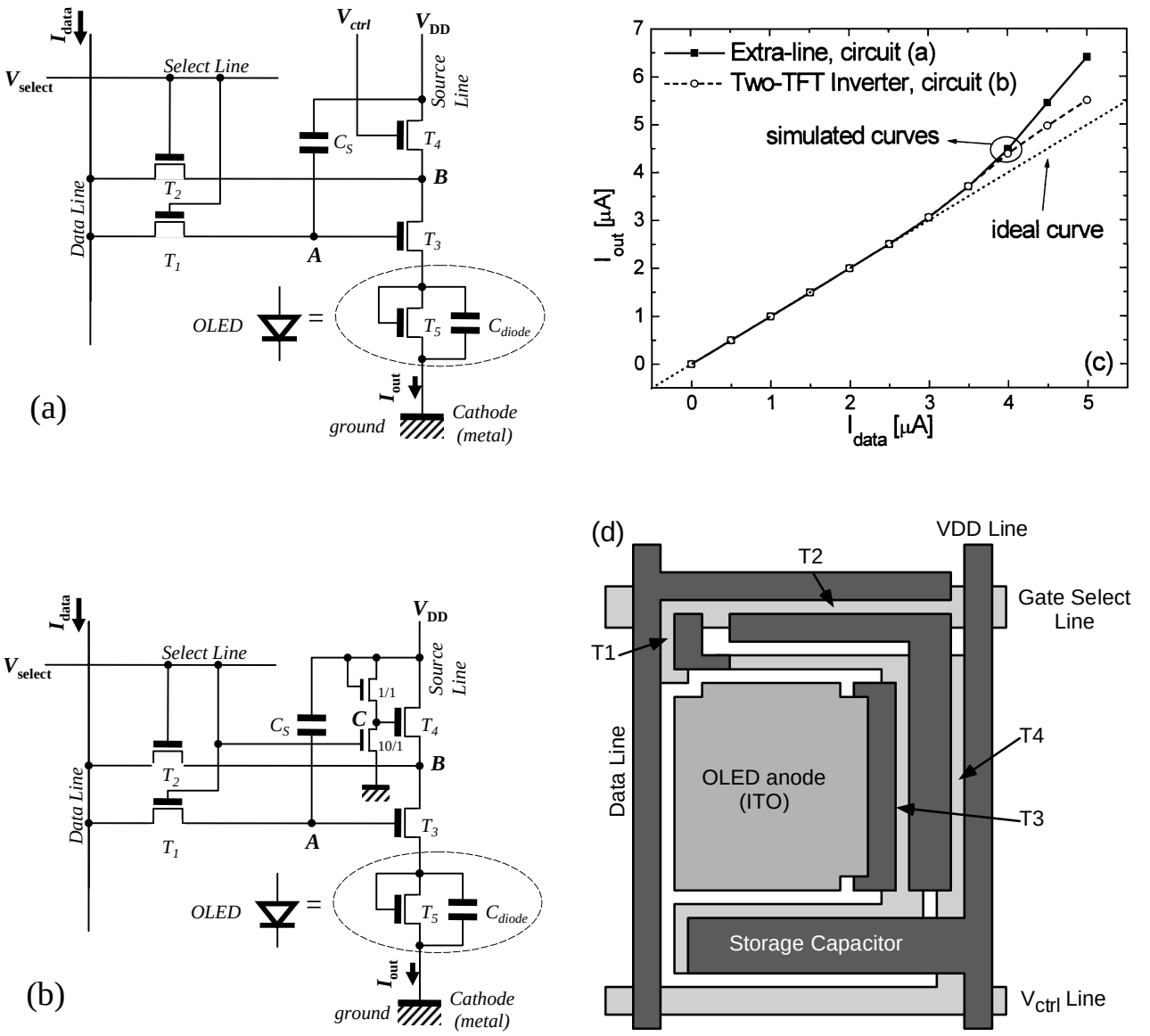

Fig. 7. (a) Constant current-source, four-TFT pixel electrode circuit using an extra voltage terminal (V_{ctrl}). (b) Constant current-source pixel electrode circuit using a two-TFT based inverter. (c) Pixel electrode circuit simulation results for the two pixel electrode circuits given in (a) and (b). (d) Top view of the four-TFT pixel electrode circuit using an extra voltage terminal (V_{ctrl}). TFTs labeled 1/1 and 10/1 are T6 and T7, respectively. The label represents their W/L ratio in units of μm.

Table III. Summary of the simulation parameters used for calculation of Fig. 7(c).

W_1/L_1	W_2/L_2	W_3/L_3	W_4/L_4	W_5/L_5	W_6/L_6	W_7/L_7
50/6 μ	100/6 μm	250/6 μm	250/6 μm	200/6 μm	1/6 μm	10/6 μm
V_{DD}	V_{select}	V_{ctrl}	I_{data}	C_{diode}	C_s	R_s	C_p
25 V	$0 \rightarrow 25$ V	$25 \rightarrow 0$ V	$0 \rightarrow 5$ μA	6.4 pF	6.61 pF	100 Ω	570 fF

itors (C_p) were set at 570 fF, about one order of magnitude higher than the values given above in order to achieve simulation convergence. Figure 7(c) shows the simulated output current (I_{out}) versus input current (I_{in}) characteristics for both pixel electrode circuits. In this simulation, the a-Si:H TFT density-of-state (DOS) model developed by our group was used.[9] Also, the experimental circuit parameters were used for this pixel circuit simulation. As expected, the simulation results indicate that the output currents for both pixel electrode circuits are very close to the ideal case. The output current levels differ by only less than 0.5% from the ideal case at low currents, indicating excellent I_{out}–I_{in} linearity. Moreover, a pixel output current level higher than 5 μA can be achieved with these pixel electrode circuits. For an 11-inch VGA full-color AM-OLED with a pixel electrode size of $\sim 100 \times 200\,\mu m^2$, this output current level is equivalent to a current density of 25 mA/cm^2. Assuming the OLEDs with an external quantum efficiency of 1%, the display brightness

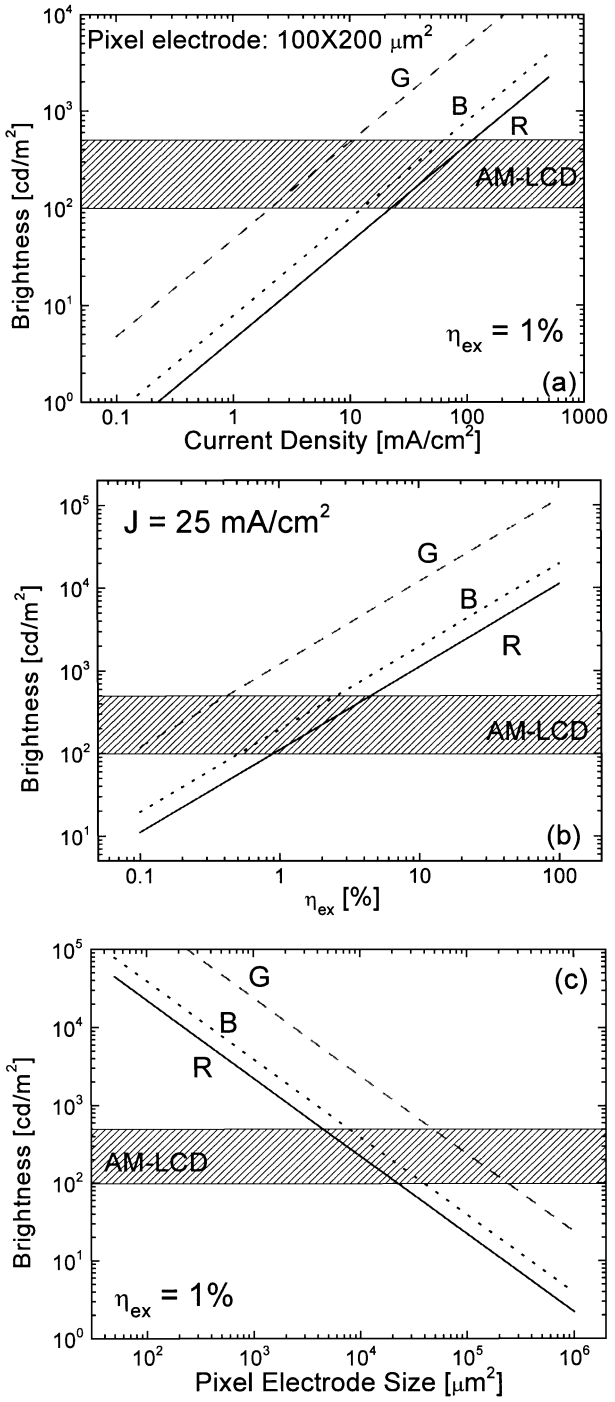

Fig. 8. OLED brightness as a function of (a) current density ($\eta_{ex} = 1\%$), (b) OLED external quantum efficiency ($J = 25\,\mathrm{mA/cm^2}$), and (c) pixel electrode size ($\eta_{ex} = 1\%$ and $I = 5\,\mu\mathrm{A}$) for R, G, B emissions saturated at 650 nm, 540 nm, and 480 nm, respectively.

of ~ 110, ~ 1200, and $\sim 200\,\mathrm{cd/m^2}$ for red (650 nm), green (540 nm), and blue (480 nm) light emission, respectively, can be achieved [Fig. 8(a)]. In Fig. 8(b), the display brightness as a function of OLED external quantum efficiency is shown for an applied pixel current density of $25\,\mathrm{mA/cm^2}$. In Fig. 8(c), the display brightness for different pixel electrode sizes is shown. These brightness values were calculated using the following equation:

$$L = 683E(\lambda)\eta_{ex}\frac{hc}{\pi\lambda}\frac{J}{e},$$

where L is brightness; $E(\lambda)$ is the luminous efficiency of light with wavelength of λ, with $E(650\,\mathrm{nm}) = 0.107$, $E(540\,\mathrm{nm}) = 0.954$, $E(480\,\mathrm{nm}) = 0.139$ values used in this work; J is the applied current density; η_{ex} is the device external quantum efficiency, e is the electron charge, c is the velocity of light, and h is Planck's constant. It is clear from these figures that the calculated brightness values are more than sufficient for most portable AM-OLED applications.

6. Conclusions

We have designed, fabricated, and analyzed a constant-current four-TFT pixel electrode circuit based on a-Si:H TFT technology for active-matrix organic light-emitting displays. Experimental results indicate that continuous pixel electrode excitation can be achieved with different pixel electrode circuits discussed in this paper. The pixel electrode circuits showed excellent electrical reliability with virtually no output current variation even when a large TFT threshold voltage shift was observed. In addition, two improved pixel electrode circuits have been proposed to achieve high output current level and good output-input characteristic linearity. With a typical OLED external quantum efficiency of 1%, the output current level of this pixel electrode circuit can achieve a pixel electrode brightness that is more than sufficient for most portable AM-OLED applications.

Acknowledgements

The authors would like to thank Mr. T. Tsukamizu, R. Tsuchiya and Dr. S. Martin for their technical assistance. This work was partially supported by the Center for Display Technology and Manufacturing at the University of Michigan, the Grant-in-Aid for Science Research (No. 11694167) from the Ministry of Education, Science, Sports and Culture of Japan, and the DARPA-ONR grant (N0014-99-1-0958).

1) C. C. Wu, S. Theiss, M. H. Lu, J. C. Sturm and S. Wagner: Tech. Dig. IEDM, 1996, p. 957.
2) M. Stewart, R. S. Howell, L. Pires, M. K. Hatalis, W. Howard and O. Prache: Tech. Dig. IEDM, 1998, p. 871.
3) T. Shimoda, H. Ohshima, S. Miyashita, M. Kimura, T. Ozawa, I. Yudasaka, S. Kanbe, H. Kobayashi, R. H. Friend, J. H. Burroughes and C. R. Towns: Proc. Asia Display'98, 1998, p. 217.
4) R. M. A. Dawson, Z. Shen, D. A. Furst, S. Connor, J. Hsu, M. G. Kane, R. G. Stewart, A. Ipri, C. N. King, P. J. Green, R. T. Flegal, S. Pearson, W. A. Barrow, E. Dickley, K. Ping, C. W. Tang, S. Van Slyke, F. Chen, J. Shi, J. C. Sturm and M. H. Lu: Symp. Dig. 1998 SID, 1998, p. 11.
5) Y. He, S. Gong, R. Hattori and J. Kanicki: Appl. Phys. Lett. **74** (1999) 2265.
6) Y. He, R. Hattori and J. Kanicki: Proc. 20th Int. Display Research Conf., 2000, p. 354.
7) C. Y. Chen and J. Kanicki: IEEE Electron Device Lett. **17** (1996) 437.
8) R. J. Baker, H. W. Li and D. E. Boyce: CMOS Circuit Design, Layout, and Simulation, IEEE Press Series on Microelectronic Systems, 1998.
9) C. Y. Chen and J. Kanicki: Proc. 26th European Solid State Device Research Conf., 1996, p. 1023.